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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,222	08/28/2003	Mohit Kapur	YOR920030306US1	6362

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,222	KAPUR ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/08/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed August 28, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Objections

Claim 9 is objected to because of the following informalities:

The phrase "the at least" does not fall under proper sentence structure. Applicant needs to omit "the." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 9-11, 12, & 17 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Schmidt et al. US Patent no. 4,627,057.

As per claim 1:

Schmidt et al. teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the method comprising the steps of: for a given clock cycle (Fig 2, column 4, lines 43-48), detecting the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

As per claim 4:

Schmidt et al. teaches a method further comprising the step of detecting the non-presence of a PRBS from the device (column 6, lines 4-10).

As per claim 5:

Schmidt et al. teaches a method wherein the device is one of a communication circuit and a communication channel (Figure 1 #10, "COMPUTER").

As per claim 6:

Schmidt teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 10, column 4, lines 29-31), the apparatus comprising: a memory (Figure 1 # 37); and at least one processor coupled to the memory and operative to (Figure 1 # 12): (i) for a given clock cycle (Fig 2, column 4, lines 43-48), detect the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS

and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and (ii) prohibit propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

As per claim 9:

Schmidt et al. teaches an apparatus wherein at least one processor is further operative to detect the non-presence of a PRBS from the device (column 6, lines 4-10).

As per claim 10:

Schmidt et al. teaches an apparatus wherein the device is one of a communication circuit and a communication channel (Figure 1 #10, "COMPUTER").

As per claim 11:

Schmidt et al. teaches an article of manufacture for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), comprising a machine readable medium containing one or more programs which when executed implement the steps of (column 3, lines 1-5): for a given clock cycle (Fig 2, column 4, lines 43-48), detecting the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

As per claim 12:

Schmidt et al. teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated

by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

As per claim 17:

Schmidt teaches the apparatus further comprising a third logic detector coupled to the shift register chain for detecting the non-presence of a PRBS from the device (column 6, lines 4-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2 & 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. US Patent no. 4,627,057 and further in view of Manlick et al. US Patent no. 5,282,211

As per claim 2:

Schmidt et al. substantially teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the method comprising the steps of: for a given clock cycle (Fig 2, column 4, lines 43-48), detecting the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

Schmidt et al. does not explicitly teach the incorporation of a counter during testing.

However, Manlick et al. in an analogous art teaches a method wherein the counter is incorporated to avoid at least one of multiple errors being counted for a

single error occurrence and masking errors in the output PRBS (Figure 3b # 90 & 92, column 5, lines 10-25). It would have been obvious to one skilled in the art to use the counter element within the testing device of Schmidt, since one skilled in the art would have realized that using a counter will help keep track of the error rate per clock cycle. Further it is common knowledge in the art to use a counter, during a testing procedure to keep track of the number of errors in the circuit and for measuring the error rate.

As per claim 7:

Schmidt et al. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 10, column 4, lines 29-31), the apparatus comprising: a memory (Figure 1 # 37); and at least one processor coupled to the memory and operative to (Figure 1 # 12): (i) for a given clock cycle, detect the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and (ii) prohibit propagation of the error bit for subsequent clock cycles (column 6; claim 1f).

Schmidt et al. does not explicitly teach the incorporation of a counter during testing.

However, Manlick et al. in an analogous art teaches a method wherein the counter is incorporated to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the output PRBS (Figure 3b # 90 & 92, column 5, lines 10-25). It would have been obvious to one skilled in the art to use the

counter element within the testing device of Schmidt, since one skilled in the art would have realized that using a counter will help keep track of the error rate per clock cycle. Further it is common knowledge in the art to use a counter, during a testing procedure to keep track of the number of errors in the circuit and for measuring the error rate.

Claim 3 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. US Patent no. 4,627,057 and further in view of Gilley US Patent no. 6,215,876 B1.

As per claim 3:

Schmidt et al. substantially teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the method comprising the steps of: for a given clock cycle (Fig 2, column 4, lines 43-48), detecting the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

Schmidt et al. does not explicitly teach the correction of the error bit.

However, Gilley in an analogous art teaches a method wherein the testing procedure further comprises correcting the error bit (Figure 4 # 78, column 7, lines 1-5). It would have been obvious to one skilled in the art to correct the error bit within the testing device of Schmidt, since one skilled in the art would have realized that correcting the error bit would improve the testing procedure and make it complete.

Further it is common knowledge in the art to correct the error once it has been detected.

As per claim 8:

Schmidt et al. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 10, column 4, lines 29-31), the apparatus comprising: a memory (Figure 1 # 37); and at least one processor coupled to the memory and operative to (Figure 1 # 12): (i) for a given clock cycle, detect the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and (ii) prohibit propagation of the error bit for subsequent clock cycles (column 6, claim 1f).

Schmidt et al. does not explicitly teach the correction of the error bit.

However, Gilley in an analogous art teaches a method wherein the testing procedure further comprises correcting the error bit (Figure 4 # 78, column 7, lines 1-5). It would have been obvious to one skilled in the art to correct the error bit within the testing device of Schmidt, since one skilled in the art would have realized that correcting the error bit would improve the testing procedure and make it complete. Further it is common knowledge in the art to correct the error once it has been detected.

Claim 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. US Patent no. 4,627,057 and further in view of Jungerman US PG Pub No. 20020063553 A1.

As per claim 13:

Schmidt et al. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

Schmidt et al. does not explicitly teach the apparatus to allow enough clock cycles for the input PRBS to initialize the shift register chain.

However, Jungerman in an analogous art teaches the apparatus further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and

initialize the full length of the shift register chain (Figure 2, paragraph [0020]). It would have been obvious to one skilled in the art to initialize the apparatus in Schmidt et al.'s testing procedure since that would account for a predictable test pattern and will also detect any initial flaws in the apparatus.

As per claim 14:

Schmidt et al. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f), wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector (Figure 1 # 27 & 28).

Schmidt et al. does not explicitly teach the apparatus to allow enough clock cycles for the input PRBS to initialize the shift register chain.

However, Jungerman in an analogous art teaches the apparatus further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain (Figure 2, paragraph [0020]). It would have been obvious to one skilled in the art to initialize the apparatus in Schmidt et al.'s testing procedure since that would account for a predictable test pattern and will also detect any initial flaws in the apparatus.

As per claims 15 & 16:

Schmidt et al. substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1 # 10, column 4, lines 29-31) generated by a device in response to an input PRBS received by the device (Figure 1 # 22, column 4, lines 33-37), the apparatus comprising: a shift register chain (Figure 1 # 10); a logic gate coupled to the shift register chain and the device for detecting (Figure 1, # 25), for a given clock cycle (Fig 2, column 4, lines 43-48), the presence of an error bit in the output PRBS (Figure 1 # 15, column 4, lines 20-25), the error bit representing a mismatch between the input PRBS and the output PRBS (Figure 1 # 25, column 4, lines 38-42); and at least one logic detector coupled to the logic gate for generating (Figure 1, path 26, NOR gate), in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (column 6, claim 1f).

Schmidt et al. does not explicitly teach the apparatus to allow enough clock cycles for the input PRBS to initialize the shift register chain, an error counter and ans error count display.

However, Jungerman in an analogous art teaches the apparatus further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain (Figure 2, paragraph [0020]), an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS (Figure 1 # 124) and an error count display coupled to the error counter for displaying the error count (Figure 1 # 128). It would have been obvious to one skilled in the art to initialize the apparatus in Schmidt et al.'s testing procedure since that would account for a predictable test pattern and will also detect any initial flaws in the apparatus. Also, it would have been obvious to one skilled in the art to use the counter element within the testing device of Schmidt, and display the error count since anybody skilled in the art would have realized that using a counter will help keep track of the error rate per clock cycle. Further it is common knowledge in the art to use a counter, during a testing procedure, and display the results of the counter.

Claims 1, 6, & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jungerman US PG Pub No. 20020063553 A1 further in view of Schmidt et al. US Patent no. 4,627,057.

As per claim 1:

Jungerman substantially teaches Schmidt et al. teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), the method comprising the steps of: for a given clock cycle (Figure 1, # 112), detecting the presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

As per claim 6:

Jungerman substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), the apparatus comprising: a memory (Figure 1 # 130); and at least one processor coupled to the memory and operative to (Figure 1 # 126): (i) for a given clock cycle (Fig 1, # 112), detect the

presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

As per claim 11:

Jungerman substantially teaches an article of manufacture for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), comprising a machine readable medium containing one or more programs which when executed implement the steps of (Figure 1): for a given clock cycle (Figure 1, # 112), detecting the presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

Claims 1, 6, & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jungerman US PG Pub No. 20020065621 A1 further in view of Schmidt et al. US Patent no. 4,627,057.

As per claim 1:

Jungerman substantially teaches Schmidt et al. teaches a method of checking the accuracy of an output pseudorandom bit sequence (PRBS) (Figure 1) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), the method comprising the steps of: for a given clock cycle (Figure 1, # 112), detecting the presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

As per claim 6:

Jungerman substantially teaches an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), the apparatus comprising: a memory (Figure 1 # 130); and at least one processor coupled to the memory and operative to (Figure 1 # 126): (i) for a given clock cycle (Fig 1, # 112), detect the presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have

recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

As per claim 11:

Jungerman substantially teaches an article of manufacture for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device (Figure 1 # 108), comprising a machine readable medium containing one or more programs which when executed implement the steps of (Figure 1): for a given clock cycle (Figure 1, # 112), detecting the presence of an error bit in the output PRBS (Figure 1 # 104), the error bit representing a mismatch between the input PRBS and the output PRBS (page 2, paragraph 19).

Jungerman does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles.

However Schmidt et al. in an analogous teaches the apparatus further prohibiting propagation of the error bit for subsequent clock cycles (column 6, claim 1f). It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of Jungerman, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the masking of error and ensure that the testing apparatus continues proper operation without

involving the error bit. Further it is common knowledge in the art to correct the error bit, which can be done by prohibiting the propagation of the error bit.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 5163069 A, US Pat no. 4139147 A, and US Pat no. 6684350 B1 mention the same test method comparing pseudorandom bits are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
01/06/2006

GUY LAMARRE
PRIMARY EXAMINER